Amendments to the Specification:

Please replace paragraph **[0006]** of the substitute filed September 19, 2002 with the following amended paragraph:

[0006] As shown in FIG. 30, an etch mask 232 is patterned on the surface of the insulative barrier layer 226, such that openings 234 in the ~~first~~ etch mask 232 are located substantially over the source region 206 and the drain region 208. The insulative barrier layer 226 is then etched through openings 234 to form vias 236 which expose ~~a~~ at least a portion of the source region 206 and the drain region 208, as shown in FIG. 31. The etch mask 232 is then removed, as shown in FIG. 32. A first conductive material 238 is deposited over the insulative barrier layer 226 to fill the vias 236, as shown in FIG. 33. The first conductive material 238 is planarized, as shown in FIG. 34, to electrically separate the first conductive material 238 within each via 236 (see FIG. 33), thereby forming contacts 242. The planarization is usually performed using a mechanical abrasion process, such as chemical mechanical planarization (CMP).

Please replace paragraph **[0008]** of the substitute specification filed September 19, 2002 with the following amended paragraph:

[0008] Although methods as described above are used in the industry, it is becoming more difficult to control the proper alignment of the etch mask 232 for the formation of the contacts 242, as tolerances become more and more stringent. For example, as shown in FIGs. 39 and 40, misalignment of the etch mask 232 can occur. Thus, as shown in FIG. 40, when the insulative barrier layer 226 is etched through the misaligned etch mask 232 to form a first via 256 and a second via 258, the etch forming the first via 256 can destroy a portion of the transistor insulating spacer member 222 and/or the cap insulator 224 to expose the gate conducting layer 218 of the transistor gate member 212. Thus, when a conductive material (not shown) is deposited in the first via 256, the gate conducting layer 218 will short, rendering the transistor ineffectual. Furthermore, the misaligned etch mask 232 can also result in the second via 258

exposing a portion of the thick field oxide area 204. However, since the etch to form the second via 258 is generally an oxide insulator-type etch, the etch may also etch through the thick field oxide area 204 to form a third via 262, thereby exposing a portion of the semiconductor substrate 202. Thus, when a conductive material (not shown) is deposited in the second via 258, the conductive material may short with the exposed portion of the semiconductor substrate 202.